Printed Page:- 04 **Subject Code:- ACSE0304 / ACSEH0304**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B. Tech

SEM: III - THEORY EXAMINATION - (2023 - 2024)

Subject: Digital Logic & Circuit Design

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

1-a. 1's complement of Binary number 101010 is____. (CO1) 1

(a) 10101
(b) 11011
(c) 1000
(d) 101011

1-b. _____ is called Universal Gate.(CO1) 1

(a) XOR Gate
(b) XNOR Gate
(c) NAND Gate
(d) AND Gate

1-c. A half adder circuit has two inputs and (CO2) 1

(a) one output
(b) two output
(c) three output
(d) none of these

1-d. If there are n selection lines, then the number of maximum possible input lines is ____. (CO2) 1

(a) 2^n
(b) n

(c) 2n

(d) n/2

1-e. The basic latch consists of _____ (CO3) 1

(a) Two inverters

(b) Two comparators

(c) Two amplifiers

(d) Two adders

1-f. Number of flip-flops required in MOD 5 counter. (CO3) 1

(a) 2

(b) 3

(c) 4

(d) 5

1-g. How many flip-flops are required to construct a decade counter? (CO4) 1

(a) 4

(b) 8

(c) 5

(d) 10

1-h. In which model, the next state is a function of the present state and the present inputs. Its output is also a function of the present state and the present inputs. (CO4) 1

(a) Mealy Circuit model

(b) Moore Circuit Model

(c) Both of these

(d) None of these

1-i. The full form of ROM is _____ (CO5) 1

(a) Read Outside Memory

(b) Read Out Memory

(c) Read Only Memory

(d) Read One Memory

1-j. PLDs with programmable AND and fixed OR arrays are called _____. (CO5) 1

(a) PAL

(b) PLA

(c) APL

(d) PPL

2. Attempt all parts:-

2.a. List out the truth table entry for two input NAND Gate.(CO1) 2

2.b. Define Multiplexer. (CO2) 2

2.c.	Differentiate between edge triggering and level triggering. (CO3)	2
2.d.	Define propagation delay time. (CO4)	2
2.e.	Differentiate between ROM and RAM. (CO5)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Construct the Hamming code for the 4 bit data 1010. Consider the even parity. (CO1)	6
3-b.	Implement the Boolean expression F(A,B,C) = ABC'+ A'B'+ AC' using both universal logic gates. (CO1)	6
3-c.	Implement the SUM and CARRY Boolean functions of full adder using multiplexers. (CO2)	6
3-d.	What is the logic implementation of half adder? Implement full adder using half adders. (CO2)	6
3.e.	What is a master-slave flip-flop? Explain its working with suitable diagram. (CO3)	6
3.f.	Difference between synchronous and asynchronous sequential circuits. (CO4)	6
3.g.	Differentiate and compare FPGA and CPLD. (CO5)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Minimize the given four variable logic function using Quine Mc-Clusky Method:- (CO1) F(A, B, C, D) = Σm (0,1, 2, 3,5, 7, 8, 9, 11, 14)	10
4-b.	Simplify the logic expression using K map:- (CO1) F(A, B, C, D, E) = Σm(0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27, 29, 31)	10

5. Answer any one of the following:-

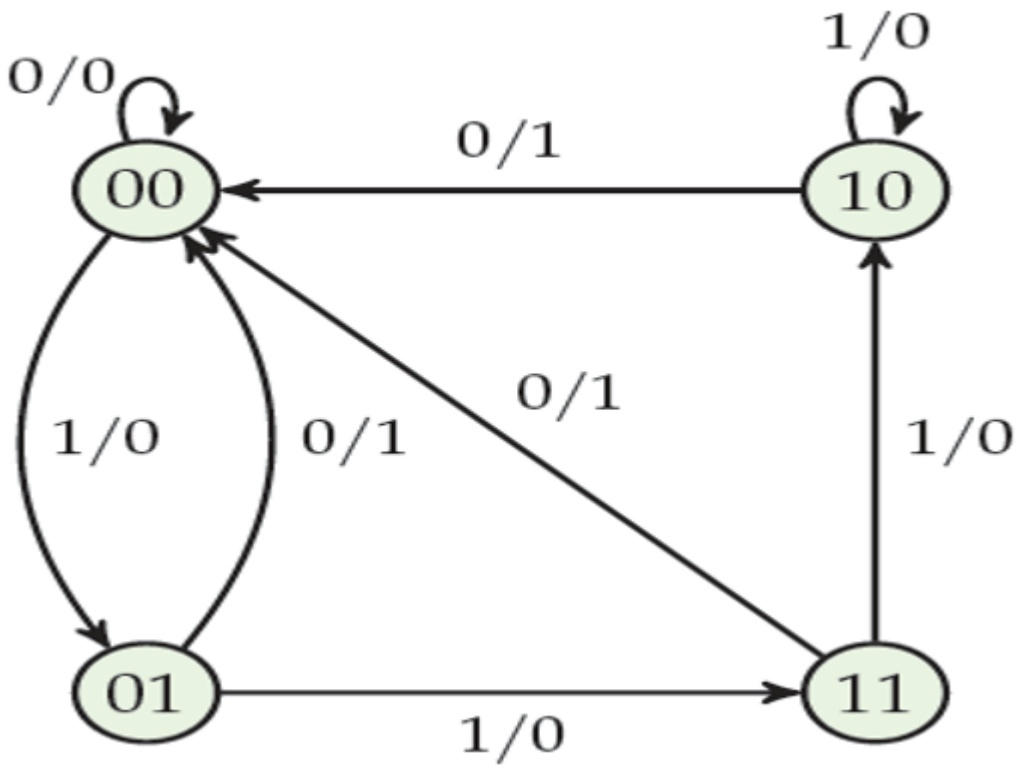
5-a.	Design a combinational circuit that will compare two 4-bit numbers. (CO2)	10
5-b.	Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number. (CO2)	10

6. Answer any one of the following:-

6-a.	What is a flip-flop? Convert SR flip flop to D flip flop. (CO3)	10
6-b.	Explain universal shift register in detail. (CO3)	10

7. Answer any one of the following:-

7-a.	Explain Hazards in sequential circuits. (CO4)	10
7-b.	Draw the reduced state table and reduce state diagram for the state diagram shown in fig. (CO4)	10



8. Answer any <u>one</u> of the following:-

8-a. Implement the following functions using PLA (CO5) 10

i) A(x,y,z)=$\sum m(1,2,4,6)$

ii) B(x,y,z)=$\sum m(0,1,6,7)$

iii) C(x,y,z)=$\sum m(2,6)$

8-b. Compare various programmable devices. (CO5) 10